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09/706,154	11/03/2000	Marlo Nemirovsky	P3816	5008

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EXAMINER	
GERSTL, SHANE F	
ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/706,154	NEMIROVSKY ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 and 6-12 have been examined.

Papers Received

2. Receipt is acknowledged of extension of time, amendment, and letter to draftsperson papers submitted, where the papers have been placed of record in the file.

Response to Amendment

3. The previous rejection set forth on the action mailed 24 September 2003, based on 35 U.S.C. 112 second paragraph, to claim 4 has been overcome by the amendment and is thus withdrawn.

4. The previous objections set forth on the action mailed 24 September 2003 to claims 1, 3, 5-6, 9, 11, and 12 have been overcome by the amendment and are thus withdrawn. The objection to claim 7 regarding the decoupling of fetching has also been withdrawn.

5. The objection to claim 7 based on "an instruction queue " still stands and is further described below.

6. The previous objections set forth on the action mailed 24 September 2003 to the specification, title, and drawings, have been overcome by the amendment and are thus withdrawn.

Response to Arguments

7. Applicant's arguments, see pages 9-11, filed January 9, 2004, with respect to the rejection(s)of claim(s) 1-12 under 35 U.S.C. 102 have been fully considered and are

persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Parady (5,933,627).

Claim Objections

8. Claim 7 is objected to because of the following informalities: as stated in the previous action, lines 1-2 of the claim state that there is "an instruction queue." Line 4 states that "a set of instruction queues" are placed in the processor. Since only one instruction queue had been previously defined, the examiner cannot determine whether the set of queues is referring to the same one queue or not. Based on the specification and figure 3, the applicant notes that there is a set of instruction queues but no other separate instruction queue. Therefore, the examiner is taking lines 1-2 of the claim to read "a set of instruction queues" and line 4 to read "placing the set of instruction queues."

9. Claim 12 is objected to because of the following informalities: the claim mentions that the execution units comprise "two memory ports." It is well known to one of ordinary skill in the art that a memory port is a medium to a memory structure that allows for communication with the memory. This is not an execution unit. The examiner is taking the claim to read "two memory units" in order to keep consistent with claim 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 7-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claim 7 recites the limitation "the instruction source" in line 5. There is insufficient antecedent basis for this limitation in the claim. No instruction source other than the instruction queues has been defined as of yet. The examiner is taking the claim to read "an instruction source" based on the specification.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Parady (5,933,627).

15. In regard to claim 1, Paraday discloses a pipelined multistreaming processor, comprising:

a. an instruction source; Figure 1 shows a microprocessor with an instruction cache (instruction source) that is modified to incorporate Parady's invention as stated in column 2, lines 45-47.

b. a plurality of streams enabled to fetch instructions at different times from the instruction source; Column 3, lines 50-53 show that there are four threads

that fetch instructions at different times based on which thread address is pointed to.

c. a dispatch stage for selecting and dispatching instructions to a set of execution units (figure 3, element 28);

d. a set of instruction queues having one queue associated with each stream in the plurality of streams, and located in the pipeline between the instruction source and the dispatch stage; Figure 3 shows four instruction buffers (102, 104, 106, and 108), or instruction queues, with one associated with each thread (stream), located between the dispatch stage and decode unit. Figure 1 shows that the instruction source (cache) sends instructions to the decode unit and thus the queues are between the instruction source and dispatch unit. Column 3, lines 38-40 further show that the buffers (queues) are each for a different thread.

e. a select system for selecting streams in each cycle to fetch instructions from the source; Column 3, lines 50-65 show that the particular thread (stream) address pointed to is the address that instructions are fetched from. The reference goes on to say that a thread switching (selection) logic switches between threads.

f. wherein the select system selects a number of streams for which to fetch instructions, which are fewer in number than the number of streams in the plurality of streams. It is shown that the aforementioned embodiment selects a single thread for fetching. Another embodiment given in column 4, lines 9-11 shows that round-robin thread switching between two PA registers (which hold

the stream addresses) is used, which means that one thread (stream) is selected at a time for fetching. In both cases the number of streams fetching, one, is less than the total number of streams shown in figure 3, four.

16. In regard to claim 7, Parady discloses in a pipelined multistreaming processor (figures 1 and 3) having a set of instruction queues (figure 3, elements 102, 104, 106, and 108, instruction buffers), a method for disassociating fetching from a dispatch stage, comprising the steps of:

a. Placing the set of instruction queues, one instruction queue for each stream, in the pipeline between the instruction source and the dispatch stage; Figure 3 shows four instruction buffers (102, 104, 106, and 108), or instruction queues, with one associated with each thread (stream), located between the dispatch stage and decode unit. Figure 1 shows that the instruction source (cache) sends instructions to the decode unit and thus the queues are between the instruction source and dispatch unit. Column 3, lines 38-40 further show that the buffers (queues) are each for a different thread.

b. Selecting one or more streams, fewer than the number of streams in the multistreaming processor, for which to fetch instructions in each cycle from an instruction source. Column 3, lines 50-65 show that the particular thread (stream) address pointed to is the address that instructions are fetched from. The reference goes on to say that a thread switching (selection) logic switches between threads. It is shown that this embodiment selects a single thread for fetching. Another embodiment given in column 4, lines 9-11 shows that round-

robin thread switching between two PA registers (which hold the stream addresses) is used, which means that one thread (stream) is selected at a time for fetching. In both cases the number of streams fetching, one, is less than the total number of streams (threads) shown in figure 3, four.

17. In regard to claim 11, Parady discloses the method of claim 7 wherein the dispatch stage dispatches instructions to a set of execution units. Figures 1 and 3 show that the dispatch stage sends or dispatches instructions to the a set of execution units.

18. In regard to claim 12, Emer discloses the method of claim 11 wherein the set of execution units comprises eight Arithmetic-Logic Units (ALS), and two memory ports. It is well known to one of ordinary skill that an execution unit is inherently known as a functional unit. Therefore, each of the ALUs and memory ports are functional units. The indication by Emer of multiple functional units (figure 2, element 34) includes the limitation of these ten functional units disclosed in the claim.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 2-4 and 8-are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady in view of Emer (6,470,443).

21. In regard to claim 2,

a. Parady discloses the processor of claim 1. Parady also discloses support in column 4, lines 13-14 for different numbers of threads than four.

b. Parady does not explicitly show wherein the number of streams in the plurality of streams is eight, and the number of streams selected for which to fetch instructions in each cycle is two.

c. Emer has taught wherein the number of streams in the plurality of streams is eight, and the number of streams selected for which to fetch instructions in each cycle is two. Figures 8A and 8B and column 12, line 22 to column 13, line 60 show eight threads (PC_A – PC_H) where two addresses are selected for fetching from the instruction cache (source).

d. Column 12, lines 22-24, show that the embodiment of figure 8A allows for instructions to be fetched from two threads in a single cycle. This inherently provides support for parallel processing, which speeds up performance, and greater flexibility using the two instructions. This potential for system speedup and flexibility would have motivated one of ordinary skill in the art to modify the design of Parady to use the thread selection mechanism taught by Emer.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Parady to incorporate the thread selection and instruction fetching mechanism of Emer so that multiple instructions may be fetched in a single cycle thus inducing system speedup and flexibility.

22. In regard to claim 3, Parady in view of Emer discloses the processor of claim 2 wherein the select system monitors a set of fetch program counters (FPC) having one

FPC associated with each stream, and directs fetching of instructions beginning at addresses according to the program counters. Column 3, lines 50-53 of Parady show that there is a program address register (fetch program counter) that gives the address to begin fetching from for each thread (stream).

23. In regard to claim 4, Parady in view of Emer discloses the processor of claim 2 wherein each stream selected to fetch is directed to fetch eight instructions from an instruction source. Emer has shown in column 4, lines 1-6 shows that the fetch unit of use provides at least one address to select eight instructions per cycle, where each address is a thread or stream.

24. In regard to claim 8,

a. Parady discloses the processor of claim 1. Parady also discloses support in column 4, lines 13-14 for different numbers of threads than four.

b. Parady does not explicitly show wherein the number of streams in the plurality of streams is eight, and the number of streams selected for which to fetch instructions in each cycle is two.

c. Emer has taught wherein the number of streams in the plurality of streams is eight, and the number of streams selected for which to fetch instructions in each cycle is two. Figures 8A and 8B and column 12, line 22 to column 13, line 60 show eight threads (PC_A – PC_H) where two addresses are selected for fetching from the instruction cache (source).

d. Column 12, lines 22-24, show that the embodiment of figure 8A allows for instructions to be fetched from two threads in a single cycle. This inherently

provides support for parallel processing, which speeds up performance, and greater flexibility using the two instructions. This potential for system speedup and flexibility would have motivated one of ordinary skill in the art to modify the design of Parady to use the thread selection mechanism taught by Emer.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Parady to incorporate the thread selection and instruction fetching technique of Emer so that multiple instructions may be fetched in a single cycle thus inducing system speedup and flexibility.

25. In regard to claim 9, Parady in view of Emer discloses the method of claim 8 wherein the select system monitors a set of fetch program counters (FPC) having one FPC associated with each stream, and directs fetching of instructions beginning at addresses according to the program counters. Column 3, lines 50-53 of Parady show that there is a program address register (fetch program counter) that gives the address to begin fetching from for each thread (stream).

26. In regard to claim 10,

a. Parady discloses the method claim 7

b. Parady does not disclose wherein each stream selected to fetch is directed to fetch eight instructions from an instruction source. Parady fetches four instructions per thread as shown in figure 1.

c. Emer has disclosed wherein each stream selected to fetch is directed to fetch eight instructions from an instruction source (column 4, lines 1-6).

d. This section of Emer also shows that these eight instructions are fetched all in the same cycle. This inherently provides support for parallel processing, which speeds up performance, and greater flexibility using in how the instructions are used. This potential for system speedup and flexibility would have motivated one of ordinary skill in the art to modify the design of Parady to use the thread selection mechanism taught by Emer.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Parady to incorporate multiple instruction-fetching technique of Emer so that multiple instructions may be fetched in a single cycle thus inducing system speedup and flexibility.

27. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady.

28. In regard to claim 6,

a. Parady discloses the processor of claim 1. Parady discloses in figure 1 seven ALU execution units (34, 36, 38, 40, 42, 44, 46) and one memory unit (32).

b. Parady does not explicitly teach an eighth Arithmetic-Logic Unit, and second memory unit.

c. The eight ALUs and two memory units of the claim are not described in terms of their specific functionality. With the current description, one of ordinary skill in the art would recognize only that the memory units are for use with memory and the ALUs are for use with arithmetic-logic functions. The inclusion of an eighth arithmetic-logic unit and a second memory unit to perform the same

function as the seven arithmetic logic units and one memory unit respectively provides no new or unexpected result over the prior art. Therefore, one of ordinary skill in the art would have found it obvious to duplicate an arithmetic-logic unit and the memory unit, creating an eight arithmetic-logic unit and a second memory unit for executing instructions in a multithreaded architecture. (see MPEP 2144, In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

29. In regard to claim 12,

a. Parady discloses the method of claim 11. Parady discloses in figure 1 seven ALU execution units (34, 36, 38, 40, 42, 44, 46) and one memory unit (32).

b. Parady does not explicitly teach an eighth Arithmetic-Logic Unit, and second memory unit.

c. The eight ALUs and two memory units of the claim are not described in terms of their specific functionality. With the current description, one of ordinary skill in the art would recognize only that the memory units are for use with memory and the ALUs are for use with arithmetic-logic functions. The inclusion of an eighth arithmetic-logic unit and a second memory unit to perform the same function as the seven arithmetic logic units and one memory unit respectively provides no new or unexpected result over the prior art. Therefore, one of ordinary skill in the art would have found it obvious to duplicate an arithmetic-logic unit and the memory unit, creating an eight arithmetic-logic unit and a second memory unit for executing instructions in a multithreaded architecture.

(see MPEP 2144, In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

Conclusion

30. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The patents cited in the previous office action mailed on 24 September 2003 remain pertinent to further show the art with respect to multistream selection and instruction queues.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
March 9, 2004

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